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EXAMINER	
PARK, EDWARD	

ART UNIT	PAPER NUMBER
2624	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	**Application No.**	**Applicant(s)**	
	10/813,834	TOUNAI, KEIICHIRO	
	Examiner	**Art Unit**	
	EDWARD PARK	2624	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 April 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 4/21/10 has been entered.

Response to Arguments

2. Applicant's arguments with respect to claims 1, 8, 15, have been considered but are moot in view of the new ground(s) of rejection. Applicant argues that the prior art of record does not disclose quantity ... first pattern in the second area (see pg. 10, second paragraph - pg. 11, second paragraph). This argument is not considered persuasive since the cited claims are rejected under a new ground(s) of rejection necessitated by applicant's amendment and the rejections and arguments can be seen within this action.

Regarding claims 4, 5, 11, 12, 18, 19, 21-26, applicant argues that the claims are allowable due to the same reasons as stated within the independent claims (see pg. 11, third paragraph). This argument is not considered persuasive since the independent claims are rejected and the arguments and rejections can be seen within this action.

Regarding claims 2, 3, 9, 10, 16, 17, applicant argues that the claims are allowable due to the dependencies from the respective independent claims (see pg. 12, first paragraph). This argument is not considered persuasive since the independent claims are rejected and the arguments and rejections can be seen within this action.

Regarding claims 6, 7, 13, 14, 20, applicant argues that the claims are allowable due to the dependencies from the respective independent claims (see pg. 12, second paragraph). This argument is not considered persuasive since the independent claims are rejected and the arguments and rejections can be seen within this action.

Claim Rejections - 35 USC § 101

3. In response to claims 1-7, 15-22, 25, 26, applicant argues that the claims meet the requirements for 35 USC 101 Tied-to-Criteria after an amendment, "a method of using a computer device" within the preamble (see pg. 10, second paragraph). This argument is not considered persuasive since the computer device or processor needs to be added within the body of the claim, not the preamble, rather after the phrase "comprising the steps of:". Examiner will maintain the 101 rejection, and advises the applicant to move newly added amendments within the body of the claim, not the preamble.

35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

The USPTO "Interim Guidelines for Examination of Patent Applications for Patent Subject Matter Eligibility" (Official Gazette notice of 22 November 2005), Annex IV, reads as follows:

> Descriptive material can be characterized as either "functional descriptive material" or "nonfunctional descriptive material." In this context, "functional descriptive material" consists of data structures and computer programs which impart functionality when employed as a computer component. (The definition of "data structure" is "a physical or logical relationship among data elements, designed to support specific data manipulation functions." The New IEEE Standard Dictionary of Electrical and Electronics Terms 308 (5th ed. 1993).) "Nonfunctional descriptive material" includes but is not limited to music, literary works and a compilation or mere arrangement of data.
>
> When functional descriptive material is recorded on some computer-readable medium it becomes structurally and functionally interrelated to the medium and will be statutory in most cases since use of technology permits the function of the descriptive material to be realized. Compare In re Lowry, 32 F.3d 1579, 1583-84, 32 USPQ2d 1031, 1035 (Fed. Cir. 1994) (claim to data structure stored on a computer readable medium that increases computer efficiency held statutory) and Warmerdam, 33 F.3d at 1360-61, 31 USPQ2d at 1759 (claim to computer having a specific data structure stored in memory held statutory product-by-process claim) with Warmerdam, 33 F.3d at 1361, 31 USPQ2d at 1760 (claim to a data structure per se held nonstatutory).
>
> In contrast, a claimed computer-readable medium encoded with a computer program is a computer element which defines structural and functional interrelationships between the computer program and the rest of the computer which permit the computer program's functionality to be realized, and is thus statutory. See Lowry, 32 F.3d at 1583-84, 32 USPQ2d at 1035.

Claims 1-7, 15-20, 21, 22, 25, 26 are rejected under 35 U.S.C. 101 as not falling within one of the four statutory categories of invention. The Federal Circuit[1], relying upon Supreme Court precedent[2], has indicated that a statutory "process" under 35 U.S.C. 101 must (1) be tied to a particular machine or apparatus, or (2) transform a particular article to a different state or thing. This is referred to as the "machine or transformation test", whereby the recitation of a particular machine or transformation of an article must impose meaningful limits on the claim's scope to impart patent-eligibility (See *Benson*, 409 U.S. at 71-72), and the involvement of the machine or transformation in the claimed process must not merely be insignificant extra-solution activity (See *Flook*, 437 U.S. at 590"). While the instant claim(s) recite a series of steps or acts to be performed, the claim(s) neither transform an article nor are positively tied to a particular machine that accomplishes the claimed method steps, and therefore do not qualify as a statutory process.

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[1] *In re Bilski*, 88 USPQ2d 1385 (Fed. Cir. 2008).

[2] *Diamond v. Diehr*, 450 U.S. 175, 184 (1981); *Parker v. Flook*, 437 U.S. 584, 588 n.9 (1978); *Gottschalk v. Benson*, 409 U.S. 63, 70 (1972); *Cochrane v. Deener*, 94 U.S. 780, 787-88 (1876).

That is, the method includes steps of applying, dividing, determining, simulating, checking, etc. is of sufficient breadth that it would be reasonably interpreted as a series of steps completely performed mentally, verbally, or without a machine. The cited claims do not positively recite any structure within the body of the claim which ties the claim to a statutory category. Furthermore, the examiner suggests that the structure needs to tie in the basic inventive concept of the application to a statutory category. Structure that ties insignificant pre or post solution activity to a statutory category is not sufficient in overcoming the 101 issue. Additionally, the limitations do not claim data that represents a physical object or substance, the data representing the physical object is not present and therefore can not be modified by the process in a meaningful or significant manner, and no meaningful and significant external, non-data depiction of a physical object or substance is produced. Thus, the limitations do not satisfy the transformation test.

[1] *In re Bilski*, 88 USPQ2d 1385 (Fed. Cir. 2008).

[2] *Diamond v. Diehr*, 450 U.S. 175, 184 (1981); *Parker v. Flook*, 437 U.S. 584, 588 n.9 (1978); *Gottschalk v. Benson*, 409 U.S. 63, 70 (1972); *Cochrane v. Deener*, 94 U.S. 780, 787-88 (1876).

Claims 8-14, 23, 24 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter as follows. Claims 8-14, 23, 24 are drawn to functional descriptive material recorded on a computer-readable medium. Normally, the claim would be statutory. However, the specification does not explicitly define computer readable medium encompassing statutory media such as optical or magnetic storage device. Therefore, according to 1351 OG 212, dated 2/23/2010, computer readable medium will be reasonably interpreted to cover both non-transitory tangible media and transitory propagating signals per se in view of the

ordinary and customary meaning of computer readable media. Furthermore, examiner notes that the cited interpretation is valid even if the specification is silent in regards to computer readable media and other such variations.

"A transitory, propagating signal … is not a "process, machine, manufacture, or composition of matter." Those four categories define the explicit scope and reach of subject matter patentable under 35 U.S.C. § 101; thus, such a signal cannot be patentable subject matter." (*In re Petrus A.C.M. Nuijten;* Fed Cir, 2006-1371, 9/20/2007).

Because the full scope of the claim as properly read in light of the disclosure encompasses non-statutory subject matter, the claim as a whole is non-statutory. The examiner suggests amending the claim to *include* the disclosed tangible computer readable media, while at the same time *excluding* the intangible media such as signals, carrier waves. Any amendment to the claim should be commensurate with its corresponding disclosure.

Examiner suggests, as seen within 1351 OG 212 dated 2/23/2010, applicant include the limitation, "non-transitory", within the cited claims to overcome the rejection and to avoid any issues of new matter.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

> having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. **Claims 1, 4, 5, 8, 11, 12, 15, 18, 19, 21-26, 27, 28** are rejected under 35 U.S.C. 103(a) as being unpatentable over Tounai (US 6,174,633 B1) in view of Taoka (US 6,350,977 B2).

Regarding **claim 1**, Tounai discloses a method of using a computer device for testing a mask pattern, the method comprising the steps of:

applying optical proximity-effect compensation to a first pattern to be tested and to be formed onto a mask layer, to thereby actually form a mask pattern of said mask layer (see col. 2, lines 24-34; correcting a photo-contiguous effect during manufacturing a semiconductor device including the steps of: designating a first region specified by a first mask pattern of a first level mask);

dividing said first pattern into a plurality of areas in accordance with a second pattern to be formed onto another mask layer (see fig. 4, col. 3, lines 30-40; interconnect 11 in a first level mask which is an interconnect layer pattern or its component, and a plug 12 in a second level mask which is a plug layer pattern or its component. In a first step, regions 15 and 16 separated from specified linear sides 13 and 14 parallel to each other by a distance "c", respectively, are formed by the computer 66);

determining sampling points on an edge of said first pattern (see fig. 4, see col. 3, lines 39-50; computer 66 locates a first and a second corners 17 and 18 of the interconnect 11 contained in the regions 15 and 16, respectively, in a second step. The computer 66 regards a side formed between the first corner 17 and the second corner 18 as a terminal node of the interconnect 11 in a third step. The side is referred to as a standard side 19. The computer 66

establishes in the first level mask a corrected mask pattern having a first and a second additional regions 23 and 24);

determining a test standard for each of said areas (see fig. 4, col. 3, lines 39-50; computer 66 establishes in the first level mask a corrected mask pattern having a first and a second additional regions 23 and 24 having projections "a" and lengths "b" in contact with the standard side 19 and one of the two adjacent sides 21 and 22 in a fourth step);

simulating a resist pattern formed on a resist by exposing said resist to a light through said mask pattern (see col. 2, lines 13-18, 34-40; correcting a photo-contiguous effect during manufacture of a semiconductor device); and

checking whether a dimensional gap between said first pattern and said resist pattern at each of said sampling points is within a test standard associated with an area to which each of said sampling points belongs (see col. 3, lines 39-50; computer 66 establishes in the first level mask a corrected mask pattern having a first and a second additional regions 23 and 24 having projections "a" and lengths "b" in contact with the standard side 19 and one of the two adjacent sides 21 and 22 in a fourth step), wherein a test standard for a first area among said areas and a test standard for a second area among said areas are different from each other (see fig. 4, col. 3, lines 30-50; regions 15 and 16 separated from specified linear sides 13 and 14 parallel to each other by a distance "c", respectively, are formed by the computer 66; regions 23 and 24 having projections "a" and lengths "b" in contact with the standard side 19). Tounai does not teach wherein the quantity of sampling points on the edge of said first pattern in the first area is different than the quantity of sampling points on the edge of said first pattern in the second area.

Taoka, in the same field of endeavor, teaches wherein the quantity of sampling points on the edge of said first pattern in the first area is different than the quantity of sampling points on the edge of said first pattern in the second area (see fig. 24, col. 3, lines 1-20; reduce the number of sampling points and increase the processing speed by setting the sampling points 3 on the pattern edges 1a selectively in accordance with presence/absence of the adjacent layout pattern 8 and the layout pattern 7 in another layer and conditions relating to corners etc. and causing simulation results of the sampling points 3 to represent values of the entire edges).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify Tounai to utilize different number of sampling points as suggested by Taoka, in order to enhance functionality of detecting pattern distortion by increasing the processing capabilities and speed by reducing the amount of sample points (see col. 3, lines 1-20).

Regarding **claim 4**, Tounai discloses pattern for forming a wiring layer, said second pattern is a pattern for forming a contact reaching said wiring layer, and said first area includes a third area including a contact area in which said contact makes contact with said wiring layer (see fig. 5, col. 4, lines 13-55).

Regarding **claim 5**, Tounai discloses a contact area and an ambient area surrounding said contact area (see fig. 5, col. 4, lines 13-55).

Regarding **claim 8**, Tounai discloses a computer-readable medium storing a program for causing a computer to carry out a method of testing a mask pattern (see fig. 3, lines 30-50), wherein said method is executed by said computer in accordance with said program including the steps of:

applying optical proximity-effect compensation to a first pattern to be tested and to be formed onto a mask layer, to thereby actually form a mask pattern of said mask layer (see col. 2, lines 24-34; correcting a photo-contiguous effect during manufacturing a semiconductor device including the steps of: designating a first region specified by a first mask pattern of a first level mask);

dividing said first pattern into a plurality of areas in accordance with a second pattern to be formed onto another mask layer (see fig. 4, col. 3, lines 30-40; interconnect 11 in a first level mask which is an interconnect layer pattern or its component, and a plug 12 in a second level mask which is a plug layer pattern or its component. In a first step, regions 15 and 16 separated from specified linear sides 13 and 14 parallel to each other by a distance "c", respectively, are formed by the computer 66);

determining sampling points on an edge of said first pattern (see fig. 4, see col. 3, lines 39-50; computer 66 locates a first and a second corners 17 and 18 of the interconnect 11 contained in the regions 15 and 16, respectively, in a second step. The computer 66 regards a side formed between the first corner 17 and the second corner 18 as a terminal node of the interconnect 11 in a third step. The side is referred to as a standard side 19. The computer 66 establishes in the first level mask a corrected mask pattern having a first and a second additional regions 23 and 24);

determining a test standard for each of said areas (see fig. 4, col. 3, lines 39-50; computer 66 establishes in the first level mask a corrected mask pattern having a first and a second additional regions 23 and 24 having projections "a" and lengths "b" in contact with the standard side 19 and one of the two adjacent sides 21 and 22 in a fourth step);

simulating a resist pattern formed on a resist by exposing said resist to a light through said mask pattern (see col. 2, lines 13-18, 34-40; correcting a photo-contiguous effect during manufacture of a semiconductor device); and checking whether a dimensional gap between said first pattern and said resist pattern at each of said sampling points is within a test standard associated with an area to which each of said sampling points belongs (see col. 3, lines 39-50; computer 66 establishes in the first level mask a corrected mask pattern having a first and a second additional regions 23 and 24 having projections "a" and lengths "b" in contact with the standard side 19 and one of the two adjacent sides 21 and 22 in a fourth step), wherein a test standard for a first area among said areas and a test standard for a second area among said areas are different from each other (see fig. 4, col. 3, lines 30-50; regions 15 and 16 separated from specified linear sides 13 and 14 parallel to each other by a distance "c", respectively, are formed by the computer 66; regions 23 and 24 having projections "a" and lengths "b" in contact with the standard side 19). Tounai does not teach wherein the quantity of sampling points on the edge of said first pattern in the first area is different than the quantity of sampling points on the edge of said first pattern in the second area.

Taoka, in the same field of endeavor, teaches wherein the quantity of sampling points on the edge of said first pattern in the first area is different than the quantity of sampling points on the edge of said first pattern in the second area (see fig. 24, col. 3, lines 1-20; reduce the number of sampling points and increase the processing speed by setting the sampling points 3 on the pattern edges 1a selectively in accordance with presence/absence of the adjacent layout pattern 8 and the layout pattern 7 in another layer and conditions relating to corners etc. and causing simulation results of the sampling points 3 to represent values of the entire edges).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify Tounai to utilize different number of sampling points as suggested by Taoka, in order to enhance functionality of detecting pattern distortion by increasing the processing capabilities and speed by reducing the amount of sample points (see col. 3, lines 1-20).

Regarding **claim 11**, Tounai discloses pattern for forming a wiring layer, said second pattern is a pattern for forming a contact reaching said wiring layer, and said first area includes a third area including a contact area in which said contact makes contact with said wiring layer (see fig. 5, col. 4, lines 13-55).

Regarding **claim 12**, Tounai discloses a contact area and an ambient area surrounding said contact area (see fig. 5, col. 4, lines 13-55).

Regarding **claim 15**, Tounai discloses a method using a computer device for forming a mask having a desired mask pattern, the method including the steps of:

applying optical proximity-effect compensation to a first pattern to be tested and to be formed onto a mask layer, to thereby actually form a mask pattern of said mask layer (see col. 2, lines 24-34; correcting a photo-contiguous effect during manufacturing a semiconductor device including the steps of: designating a first region specified by a first mask pattern of a first level mask);

dividing said first pattern into a plurality of areas in accordance with a second pattern to be formed onto another mask layer (see fig. 4, col. 3, lines 30-40; interconnect 11 in a first level mask which is an interconnect layer pattern or its component, and a plug 12 in a second level mask which is a plug layer pattern or its component. In a first step, regions 15 and 16 separated

from specified linear sides 13 and 14 parallel to each other by a distance "c", respectively, are formed by the computer 66);

determining sampling points on an edge of said first pattern (see fig. 4, see col. 3, lines 39-50; computer 66 locates a first and a second corners 17 and 18 of the interconnect 11 contained in the regions 15 and 16, respectively, in a second step. The computer 66 regards a side formed between the first corner 17 and the second corner 18 as a terminal node of the interconnect 11 in a third step. The side is referred to as a standard side 19. The computer 66 establishes in the first level mask a corrected mask pattern having a first and a second additional regions 23 and 24);

determining a test standard for each of said areas (see fig. 4, col. 3, lines 39-50; computer 66 establishes in the first level mask a corrected mask pattern having a first and a second additional regions 23 and 24 having projections "a" and lengths "b" in contact with the standard side 19 and one of the two adjacent sides 21 and 22 in a fourth step);

simulating a resist pattern formed on a resist by exposing said resist to a light through said mask pattern (see col. 2, lines 13-18, 34-40; correcting a photo-contiguous effect during manufacture of a semiconductor device);

checking whether a dimensional gap between said first pattern and said resist pattern at each of said sampling points is within a test standard associated with an area to which each of said sampling points belongs(see col. 3, lines 39-50; computer 66 establishes in the first level mask a corrected mask pattern having a first and a second additional regions 23 and 24 having projections "a" and lengths "b" in contact with the standard side 19 and one of the two adjacent sides 21 and 22 in a fourth step); and

transferring said mask pattern onto a mask (see col. 3, lines 30-67, col. 4, lines 1-13), wherein a test standard for a first area among said areas and a test standard for a second area among said areas are different from each other (see fig. 4, col. 3, lines 30-50; regions 15 and 16 separated from specified linear sides 13 and 14 parallel to each other by a distance "c", respectively, are formed by the computer 66; regions 23 and 24 having projections "a" and lengths "b" in contact with the standard side 19). Tounai does not teach wherein the quantity of sampling points on the edge of said first pattern in the first area is different than the quantity of sampling points on the edge of said first pattern in the second area.

Taoka, in the same field of endeavor, teaches wherein the quantity of sampling points on the edge of said first pattern in the first area is different than the quantity of sampling points on the edge of said first pattern in the second area (see fig. 24, col. 3, lines 1-20; reduce the number of sampling points and increase the processing speed by setting the sampling points 3 on the pattern edges 1a selectively in accordance with presence/absence of the adjacent layout pattern 8 and the layout pattern 7 in another layer and conditions relating to corners etc. and causing simulation results of the sampling points 3 to represent values of the entire edges).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify Tounai to utilize different number of sampling points as suggested by Taoka, in order to enhance functionality of detecting pattern distortion by increasing the processing capabilities and speed by reducing the amount of sample points (see col. 3, lines 1-20).

Regarding **claim 18**, Tounai discloses pattern for forming a wiring layer, said second pattern is a pattern for forming a contact reaching said wiring layer, and said first area includes a

third area including a contact area in which said contact makes contact with said wiring layer (see fig. 5, col. 4, lines 13-55).

Regarding **claim 19**, Tounai discloses a contact area and an ambient area surrounding said contact area (see fig. 5, col. 4, lines 13-55).

Regarding **claim 21**, Tounai discloses a gate layer, and a number of sampling points in an area acting as a gate of a transistor is higher than the same in other areas (see col. 3, lines 30-63).

Regarding **claim 22**, Tounai discloses a gate layer, and a number of sampling points in a contact area is higher than the same in other areas (see col. 3, lines 30-63).

Regarding **claim 23**, Tounai discloses a gate layer, and a number of sampling points in an area acting as a gate of a transistor is higher than the same in other areas (see col. 3, lines 30-63).

Regarding **claim 24**, Tounai discloses a gate layer, and a number of sampling points in a contact area is higher than the same in other areas (see col. 3, lines 30-63).

Regarding **claim 25**, Tounai discloses a gate layer, and a number of sampling points in an area acting as a gate of a transistor is higher than the same in other areas (see col. 3, lines 30-63).

Regarding **claim 26**, Tounai discloses a gate layer, and a number of sampling points in a contact area is higher than the same in other areas (see col. 3, lines 30-63).

Regarding **claim 27**, the claim is analyzed as an apparatus/computer device of claim 1 (see rejection of claim 1).

Regarding **claim 28**, the claim is analyzed as an apparatus/computer device of claim 15 (see rejection of claim 15).

6. **Claims 2, 3, 9, 10, 16, 17** are rejected under 35 U.S.C. 103(a) as being unpatentable over Tounai (US 6,174,633 B1) with Taoka (US 6,350,977 B2), and further in view of Tsudaka (US 5,991,006).

Regarding **claims 2, 3**, Tounai with Taoka discloses all elements as mentioned above in claim 1. Tounai with Taoka does not teach N-th sampling points located in a N-th area, among said sampling points, is determined in accordance with a N-th process in said step (c) where N indicates an integer equal to or greater than one (N = 1, 2, 3, 4, --), and first to N-th processes are different from one another; and dividing an edge of said first pattern into a plurality of portions, wherein said test standard is determined for each of said portions.

Tsudaka, in the same field of endeavor, teaches N-th sampling points located in a N-th area, among said sampling points, is determined in accordance with a N-th process in said step (c) where N indicates an integer equal to or greater than one (N = 1, 2, 3, 4, --), and first to N-th processes are different from one another (see col. 2, lines 34-67; col. 3, lines 1-15; transferred image as being closest possible to the desired design pattern in the lithography process. More specifically, the method comprises the steps of dividing the visible outline of the desired design pattern into edges according to a specified rule, then assigning a plurality of evaluation points to each of the edges; computing a transferred pattern image after the exposure by simulation; computing a distance between each evaluation point or each edge and a position corresponding to each evaluation point of the transferred image of the exposed pattern; and determining a corrected exposure pattern by inputting the distance to a specified evaluation function to correct the position of each edge according to an output value of the evaluation function. The above method of the present invention further includes the steps of dividing the visible outline of the

desired design pattern into edges according to a specified rule, then assigning a plurality of evaluation points to each of the edges; computing a transferred energy intensity of the exposed pattern by simulation; determining a corrected exposure pattern by inputting the transferred energy intensity to a specified evaluation function to correct the position of each edge according to the output value of the evaluation function; plurality of a evaluation points are assigned to each of the edges obtained by dividing the visible outline of the object design pattern and computing the distance between each evaluation point and the position corresponding to each evaluation point on the exposed pattern image, and the distance between each of a plurality of the evaluation points and the exposure image on each edge can be computed); and dividing an edge of said first pattern into a plurality of portions, wherein said test standard is determined for each of said portions (see col. 2, lines 34-67; col. 3, lines 1-15).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify the Tounai with Taoka to utilize multiple sampling points and standards as suggested by Tsudaka, in order to optimize a mask pattern for simulation and production by reducing time and processes in the correction of these irregular patterns (see col. 1, lines 20-48).

Regarding **claims 9, 10**, Tounai with Taoka discloses all elements as mentioned above in claim 8. Tounai with Taoka does not teach N-th sampling points located in a N-th area, among said sampling points, is determined in accordance with a N-th process in said step (c) where N indicates an integer equal to or greater than one (N = 1, 2, 3, 4, --), and first to N-th processes are different from one another; and dividing an edge of said first pattern into a plurality of portions, wherein said test standard is determined for each of said portions.

Tsudaka, in the same field of endeavor, teaches N-th sampling points located in a N-th area, among said sampling points, is determined in accordance with a N-th process in said step (c) where N indicates an integer equal to or greater than one (N = 1, 2, 3, 4, --), and first to N-th processes are different from one another (see col. 2, lines 34-67; col. 3, lines 1-15; transferred image as being closest possible to the desired design pattern in the lithography process. More specifically, the method comprises the steps of dividing the visible outline of the desired design pattern into edges according to a specified rule, then assigning a plurality of evaluation points to each of the edges; computing a transferred pattern image after the exposure by simulation; computing a distance between each evaluation point or each edge and a position corresponding to each evaluation point of the transferred image of the exposed pattern; and determining a corrected exposure pattern by inputting the distance to a specified evaluation function to correct the position of each edge according to an output value of the evaluation function. The above method of the present invention further includes the steps of dividing the visible outline of the desired design pattern into edges according to a specified rule, then assigning a plurality of evaluation points to each of the edges; computing a transferred energy intensity of the exposed pattern by simulation; determining a corrected exposure pattern by inputting the transferred energy intensity to a specified evaluation function to correct the position of each edge according to the output value of the evaluation function; plurality of a evaluation points are assigned to each of the edges obtained by dividing the visible outline of the object design pattern and computing the distance between each evaluation point and the position corresponding to each evaluation point on the exposed pattern image, and the distance between each of a plurality of the evaluation points and the exposure image on each edge can be computed); and dividing an

edge of said first pattern into a plurality of portions, wherein said test standard is determined for each of said portions (see col. 2, lines 34-67; col. 3, lines 1-15).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify the Tounai with Taoka to utilize multiple sampling points and standards as suggested by Tsudaka, in order to optimize a mask pattern for simulation and production by reducing time and processes in the correction of these irregular patterns (see col. 1, lines 20-48).

Regarding **claims 16, 17**, Tounai with Taoka discloses all elements as mentioned above in claim 15. Tounai with Taoka does not teach N-th sampling points located in a N-th area, among said sampling points, is determined in accordance with a N-th process in said step (c) where N indicates an integer equal to or greater than one (N = 1, 2, 3, 4, --), and first to N-th processes are different from one another; and dividing an edge of said first pattern into a plurality of portions, wherein said test standard is determined for each of said portions.

Tsudaka, in the same field of endeavor, teaches N-th sampling points located in a N-th area, among said sampling points, is determined in accordance with a N-th process in said step (c) where N indicates an integer equal to or greater than one (N = 1, 2, 3, 4, --), and first to N-th processes are different from one another (see col. 2, lines 34-67; col. 3, lines 1-15; transferred image as being closest possible to the desired design pattern in the lithography process. More specifically, the method comprises the steps of dividing the visible outline of the desired design pattern into edges according to a specified rule, then assigning a plurality of evaluation points to each of the edges; computing a transferred pattern image after the exposure by simulation; computing a distance between each evaluation point or each edge and a position corresponding to each evaluation point of the transferred image of the exposed pattern; and determining a

corrected exposure pattern by inputting the distance to a specified evaluation function to correct the position of each edge according to an output value of the evaluation function. The above method of the present invention further includes the steps of dividing the visible outline of the desired design pattern into edges according to a specified rule, then assigning a plurality of evaluation points to each of the edges; computing a transferred energy intensity of the exposed pattern by simulation; determining a corrected exposure pattern by inputting the transferred energy intensity to a specified evaluation function to correct the position of each edge according to the output value of the evaluation function; plurality of a evaluation points are assigned to each of the edges obtained by dividing the visible outline of the object design pattern and computing the distance between each evaluation point and the position corresponding to each evaluation point on the exposed pattern image, and the distance between each of a plurality of the evaluation points and the exposure image on each edge can be computed); and dividing an edge of said first pattern into a plurality of portions, wherein said test standard is determined for each of said portions (see col. 2, lines 34-67; col. 3, lines 1-15).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify the Tounai with Taoka to utilize multiple sampling points and standards as suggested by Tsudaka, in order to optimize a mask pattern for simulation and production by reducing time and processes in the correction of these irregular patterns (see col. 1, lines 20-48).

7. **Claims 6, 7, 13, 14, 20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Tounai (US 6,174,633 B1) with Taoka (US 6,350,977 B2), and further in view of Miyazaki (US 6,665,858 B2).

Regarding **claims 6, 7**, Tounai with Taoka discloses all elements as mentioned above in claim 1. Tounai with Taoka does not teach pattern for forming a wiring layer including a gate of a MOS transistor, said second pattern is a pattern for forming an active area of said MOS transistor, and said first area includes a fourth area including a fifth area obtained by projecting said active area onto said first pattern; and fifth area and an ambient area surrounding said fifth area.

Miyazaki, in the same field of endeavor, teaches pattern for forming a wiring layer including a gate of a MOS transistor, said second pattern is a pattern for forming an active area of said MOS transistor, and said first area includes a fourth area including a fifth area obtained by projecting said active area onto said first pattern (see col. 2, lines 1-17, col. 6, lines 64-67, col. 7, lines 1-21); and fifth area and an ambient area surrounding said fifth area (see col. 6, lines 64-67, col. 7, lines 1-21).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify the Tounai with Taoka to utilize a wiring layer and multiple areas as suggested by Miyazaki, in order to ensure that the simulation and production of layers/patterns are accurately in compliance with design data (see col. 1, lines 53-63).

Regarding **claims 13, 14**, Tounai with Taoka discloses all elements as mentioned above in claim 8. Tounai with Taoka does not teach pattern for forming a wiring layer including a gate of a MOS transistor, said second pattern is a pattern for forming an active area of said MOS transistor, and said first area includes a fourth area including a fifth area obtained by projecting said active area onto said first pattern; and fifth area and an ambient area surrounding said fifth area.

Miyazaki, in the same field of endeavor, teaches pattern for forming a wiring layer including a gate of a MOS transistor, said second pattern is a pattern for forming an active area of said MOS transistor, and said first area includes a fourth area including a fifth area obtained by projecting said active area onto said first pattern (see col. 2, lines 1-17, col. 6, lines 64-67, col. 7, lines 1-21); and fifth area and an ambient area surrounding said fifth area (see col. 6, lines 64-67, col. 7, lines 1-21).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify the Tounai with Taoka to utilize a wiring layer and multiple areas as suggested by Miyazaki, in order to ensure that the simulation and production of layers/patterns are accurately in compliance with design data (see col. 1, lines 53-63).

Regarding **claim 20**, Tounai with Taoka discloses all elements as mentioned above in claim 15. Tounai with Taoka does not teach pattern for forming a wiring layer including a gate of a MOS transistor, said second pattern is a pattern for forming an active area of said MOS transistor, and said first area includes a fourth area including a fifth area obtained by projecting said active area onto said first pattern.

Miyazaki, in the same field of endeavor, teaches pattern for forming a wiring layer including a gate of a MOS transistor, said second pattern is a pattern for forming an active area of said MOS transistor, and said first area includes a fourth area including a fifth area obtained by projecting said active area onto said first pattern (see col. 2, lines 1-17, col. 6, lines 64-67, col. 7, lines 1-21).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify the Tounai with Taoka to utilize a wiring layer and multiple areas as suggested

by Miyazaki, in order to ensure that the simulation and production of layers/patterns are accurately in compliance with design data (see col. 1, lines 53-63).

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to EDWARD PARK whose telephone number is (571)270-1576. The examiner can normally be reached on M-F 10:30 - 20:00, (EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Samir Ahmed can be reached on (571) 272-7413. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Edward Park
Examiner
Art Unit 2624

/Edward Park/

Examiner, Art Unit 2624
/Brian Q Le/
Primary Examiner, Art Unit 2624